The Applicants acknowledge the Examiner's indication that Claims 5 and 6 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, the Applicants have added new Claims 11 and 12 to recite the limitations that the Examiner has indicated are allowable in Claims 5 and 6, respectively.

I. Formal Matters and Objections

The Examiner has objected to the title as not being descriptive. In response, the Applicants have amended the title to correct this inadvertent error.

II. Rejection of Claim 10 under 35 U.S.C. §112

The Examiner has rejected Claim 10 under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, the Applicants have amended Claim 10 to correct this inadvertent error. Accordingly, the Applicants respectfully request the Examiner to withdraw the §112 rejection with respect to Claim 10.

III. Rejection of Claims 1-4 and 7-10 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4 and 7-10 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,265,783 to Juso, *et al.* ("Juso"). However, Juso fails to disclose a passivation layer exposing only pads of a first set, or exposing pads of the first set and a second set, as recited in Claims 1 and 8 of the present invention. Contrary to the Examiner's assertion, the insulative substrate 5 disclosed in Juso is not a passivation layer, as recited in Claims 1 and 8 of the present invention. The insulative substrate 5 disclosed in Juso cannot be a passivation layer because it has a plurality of through-holes 9 formed therein. (Column 4, lines 57-58, *et seq.*). One having ordinary skill in the pertinent art understands that passivation layers are employed in integrated circuit manufacturing as final, protective layers, and that, therefore, an insulative substrate having a plurality of through-holes therein is not a passivation layer. In addition, Juso also discloses that dummy lands 11 may be constructed to only partially cover the through-holes in the insulative substrate 5, further reinforcing the fact that the insulative substrate 5 disclosed in Juso was not intended to be a passivation layer and, in fact, cannot even function as a passivation layer.

Therefore, because Juso fails to disclose a passivation layer, Juso also fails to anticipate independent Claims 1 and 8 of the present application. Because Claims 2-4, 7 and 9-10 are dependent upon these independent Claims, Juso also fails to anticipate Claims 2-4, 7 and 9-10. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to Claims 1-4 and 7-10.

In addition, new Claims 11 and 12 are also not anticipated by Juso, because they contain limitations that the Examiner has indicated are allowable.

IV. Rejection of Claims 1-3 and 8-10 under 35 U.S.C. §102

The Examiner has rejected Claims 1-3 and 8-10 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,641,946 to Shim. However, Shim fails to disclose a first predetermined center-to-center spacing between each pad of a first set and an adjacent pad or pads of the first set, a second predetermined center-to-center spacing, less than the first spacing, between each pad of a second set and the adjacent pad or pads of the first and second sets, wherein each pad of the first set is larger than each pad of the second set, and a passivation layer exposing only pads of the first set, or exposing pads of the first and second sets, as recited in Claims 1 and 8 of the present application.

The Examiner has asserted that the insulating mask 6 disclosed in Shim is a passivation layer as recited in Claims 1 and 8 of the present application. However, in the embodiments disclosed in Shim that include the insulating mask 6, the solder ball lands 5 all have the same size. Accordingly, Shim fails to disclose both a passivation layer and first and second sets of conductive pads wherein the pads of the first set are larger than the pads of the second set, as recited in Claims 1 and 8 of the present application.

In addition, Shim also fails to disclose a second predetermined center-to-center spacing between each pad of a second set and an adjacent pad of a first set or the second set, wherein the second spacing is less than a first spacing between the pads of the first set, as recited in Claims 1 and 8 of the present application. Specifically, all of the figures in Shim depict all of the solder ball lands 5 and corresponding solder balls 3 as being uniformly spaced from one another, such that Shim fails to disclose a second spacing.

Therefore, because Shim fails to disclose a passivation layer and first and second sets of pads, and because Shim fails to disclose a second predetermined center-to-center spacing that is less than a first spacing, Shim fails to anticipate Claims 1 and 8 of the present application. Because

Claims 2-3 and 9-10 are dependent upon Claims 1 and 8, respectively, Shim also fails to anticipate Claims 2-3 and 9-10. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to Claims 1-3 and 8-10.

In addition, new Claims 11 and 12 are also not anticipated by Shim, because they contain limitations that the Examiner has indicated are allowable.

V. Rejection of Claim 1 under 35 U.S.C. §102

The Examiner has rejected Claim 1 under 35 U.S.C. §102(b) as being anticipated by European Patent No. 0481889-A1 to Pradel. However, Pradel fails to disclose a first set of pads being exposed by a passivation layer and having a spacing that is greater than the spacing of a second set of pads. To the contrary, the first set of pads (TAB blocks 14), which are exposed by the passivation layer, are closer to one another than the second set of pads 16, which have a greater spacing than the first set of pads. Therefore, Pradel fails to disclose every element of the Claims.

Therefore, Pradel fails to anticipate Claim 1. Accordingly, the Applicants respectfully request the Examiner to withdraw the §102 rejection with respect to Claim 1.

In addition, new Claims 11 and 12 are also not anticipated by Pradel, because they contain limitations that the Examiner has indicated are allowable.

VI. Rejection of Claim 7 under 35 U.S.C. §103

The Examiner has rejected Claim 7 under 35 U.S.C. §103(a) as being unpatentable over Shim. The Examiner has asserted that while Shim does not specifically disclose connecting the pads to connection points in the integrated circuit, it would have been obvious to do so for the purpose of providing electrical contacts between the semiconductor die and the mother board. However, such an assertion does not overcome Shim's shortcomings discussed above. Specifically, Shim fails to teach or suggest a passivation layer and first and second sets of pads, as well as a second predetermined center-to-center spacing that is less than a first spacing, as recited in Claim 1 of the present application. Therefore, Shims fails to support a *prima facie* case of obviousness with respect to Claim 1. Because Claim 7 is dependent upon Claim 1, Shim also fails to support a *prima facie* case of obviousness with respect to Claim 7. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103 rejection with respect to Claim 7.

In addition, Shim also fails to support a *prima facie* case of obviousness with respect to new Claims 11 and 12, because they contain limitations that the Examiner has indicated are allowable.

VII. Additional References Made of Record

The Applicants believe that the additional references made of record and not relied upon by the Examiner are not particularly pertinent to the claimed invention, but the Applicants retain the right to address these references in detail, if necessary, in the future.

VIII. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-12.

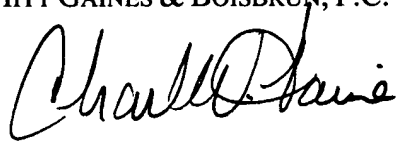
Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Commissioner is hereby authorized to charge the extra independent claim fee due of $42.00 or any additional fees connected with this communication to Deposit Account No. 08-2395.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

HITT GAINES & BOISBRUN, P.C.



Charles W. Gaines
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please amend the title of the invention as follows:

[IMPROVEMENTS IN OR RELATING TO] INTEGRATED CIRCUIT DIE[S] FOR WIRE BONDING AND FLIP-CHIP MOUNTING

IN THE CLAIMS:

(1) Please amend Claim 1 as follows:

1. (Amended) An integrated circuit die including first and second sets of conductive pads for enabling external connections to be made to the integrated circuit, wherein each pad of said first set is larger than each pad of said second set, there being at least a first predetermined center-to-center spacing between each pad of the first set and the adjacent pad or pads of the first set, and at least a second predetermined center-to-center spacing, less than said first spacing, between each pad of the second set and the adjacent pad or pads of the first and second sets, and a passivation layer exposing only pads of the first set, or exposing pads of the first and second sets.

(2) Please amend Claim 8 as follows:

8. (Amended) An integrated circuit die, comprising:

a first set of conductive pads having a first minimum distance therebetween; and

a second set of conductive pads having a second minimum distance therebetween, and between a pad of the second set and a neighboring pad of the first set, wherein each pad of said first set is larger than each pad of said second set;

wherein the die is adapted for selective use as one of a flip-chip assembly and a wire bond.

(3) Please amend Claim 10 as follows:

10. (Amended) A die as recited in claim 8, further comprising a [second] passivation layer for use of the die as a wire bond assembly.

(4) Please add new Claim 11 as follows:

--11. (New) An integrated circuit die including first and second sets of conductive pads for enabling external connections to be made to the integrated circuit, there being at least a first predetermined center-to-center spacing between each pad of the first set and the adjacent pad or pads of the first set, and at least a second predetermined center-to-center spacing, less than said first spacing, between each pad of the second set and the adjacent pad or pads of the first and second sets, wherein the pads of the first set are disposed in two lines adjacent one or more edges of the die, the pads of the first set in one of the two lines being disposed in staggered relationship with respect to the pads of the first set in the other of the two lines, and a passivation layer exposing only pads of the first set, or exposing pads of the first and second sets.--

(5) Please add new Claim 12 as follows:

--12. (New) A die as claimed in Claim 11 wherein the pads of the second set are disposed in one of the two lines.--